



#9/4-4-03
V.3024
Patent
260/085
19535-7061

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:) Group Art Unit: 2857
Bulent Dervisoglu et al.)
Serial No.: 09/765,958)
Filed: January 18, 2001)
For: HIERARCHICAL TEST CIRCUIT)
STRUCTURE FOR CHIPS WITH)
MULTIPLE CIRCUIT BLOCKS)

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Customer Number 23639
Bingham McCutchen LLP
Three Embarcadero Center, Suite 1800
San Francisco, CA 94111-4067

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with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith. Send all future correspondence to the attention of Peter C. Mei, Reg. No. 39,768, care of the above address and direct all telephone calls to the same at (650) 849-4870.

Assignee of Interest:

Cadence Design Systems, Inc.

Dated: 1/15/03

By: Peter Chen

Name: Peter Chen

Title: Vice President and

Associate General Counsel

Address of Assignee of Interest:

Cadence Design Systems, Inc.
2655 Seely Avenue
San Jose, CA 95134



2857

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Total Number Of Documents In This Submission

Application Number	09/765,958
Filing Date	January 18, 2001
First Named Inventor	Bulent Dervisoglu et al.
Group Art Unit	2857
Examiner Name	Not yet assigned

ENCLOSURES (check all that apply)

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY OR AGENT

Firm or Individual Name	Peter C. Mei Bingham McCutchen LLP Three Embarcadero Center, Suite 1800 San Francisco, CA 94111-4067
Signature	
Date	February 11, 2003

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